AN 13.18

Scalable 10/100 Ethernet Reference Design to support Migration from the SMSC LAN83C185 Non Auto-MDIX PHY to a Future SMSC LAN8187 HP Auto-MDIX PHY

1 Introduction

This application note provides guidelines to support designs which will be migrating from the LAN83C185 Non Auto-MDIX PHY to the LAN8187 HP Auto-MDIX PHY. With this migration, the HP Auto-MDIX feature of the LAN8187 can be implemented without the need to make changes to the schematics, magnetics or PCB board design. The only change required is to populate/de-populate the indicated passive components.

This Scalable Reference Design covers design considerations for analog, digital and power signals. Section 2.1, "Analog Connection Considerations," on page 2 covers the analog signal considerations while Section 2.2, "Other Considerations," on page 6 covers the digital and power signal considerations to support the migration from the LAN83C185 to the LAN8187.

HP Auto-MDIX facilitates the use of either a direct connect or cross-over CAT-3 (10 Base-T) or CAT-5 (100 Base-T) media UTP interconnect cable (Figure 1.1). The LAN8187 HP Auto-MDIX PHY is capable of detecting whether a direct connect or cross-over cable is being used and configuring the TXP/TXN and RXP/RXN pins for correct Transmit and Receive operation. The SMSC LAN83C185 device is not capable of HP Auto MDIX detection and operation. Therefore, if HP Auto MDIX is needed in the future, follow the guidelines in the application note to be prepared to take advantage of this feature.

This application note makes recommendations for reference only. The end customer's application will determine the final PCB design as there may be specific requirements which are not considered in this application note.

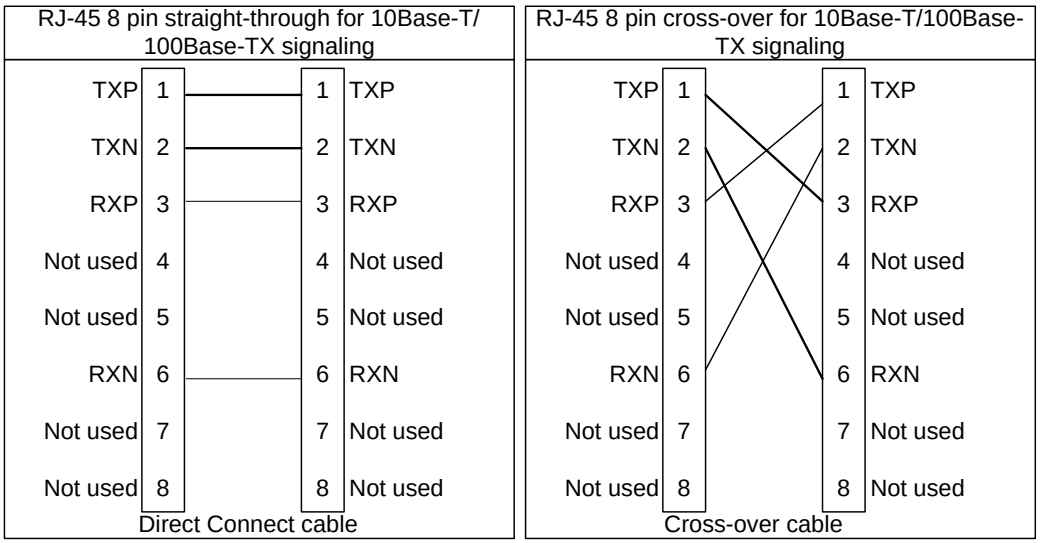

Figure 1.1 Direct Connect and Cross-Over Cabling Diagrams

2 Scalable Design Configuration for Non Auto MDIX (LAN83C185) or HP Auto MDIX (LAN8187) Operation

2.1 Analog Connection Considerations

Figure 2.1 illustrates how a complete scalable reference design would be implemented. When the PHY is populated with an SMSC LAN83C185, the designer can configure proper operation by populating the capacitors C1 and C2 with 6.8nF capacitors to allow AC signals to pass from the magnetics to the receive pins RXP and RXN. Capacitor C4 is populated to provide filtering of the center tap voltage. Also for this configuration, resistor R3 is populated with a 0 ohm resistor to tie the magnetics center tap to the RXP and RXN DC component. R7 and R8 are not used in this configuration and must be de-populated.

When the PHY is populated with an SMSC LAN8187, the designer can configure proper HP Auto MDIX operation by populating the locations C1, C2, R7, and R8 with 0 ohm resistors. C1 and C2 must be populated with 0 ohm resistors. Resistor R7 is populated with a 0 ohm resistor to connect the center taps of the transmit and receive magnetic modules together. Resistor R8 is populated with a 0 ohm resistor to bring the TX/RX pins up to 3.3 volts through a pair of 50 ohm resistors. Capacitor C4 and resistor R3 must be removed or de-populated for this configuration.

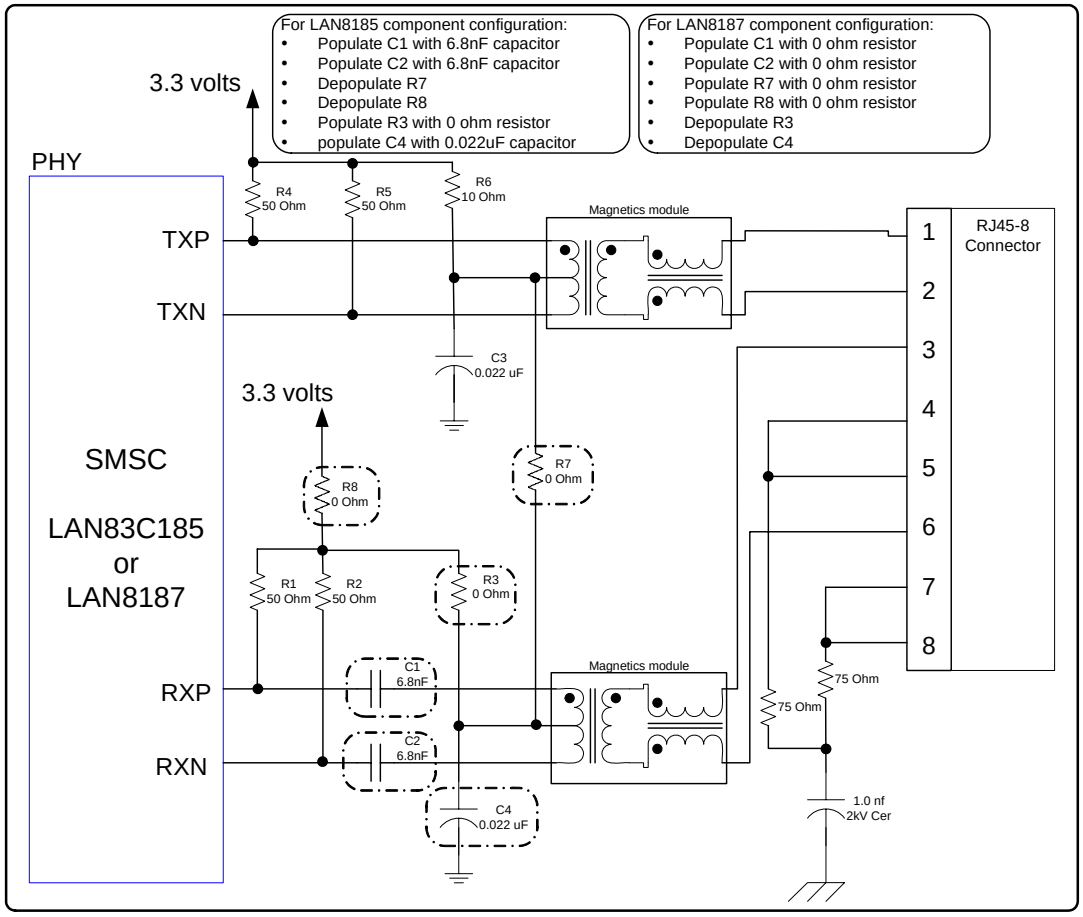

Figure 2.1 Scalable Design Configuration for the LAN83C185 with Optional HP Auto MDIX Option for a Future LAN8187

2.1.1 Scalable Design Configuration for Non Auto MDIX Mode

Figure 2.2 below illustrates how the scalable design would be configured for an SMSC LAN83C185 PHY operation. Since the LAN83C185 PHY is not capable of HP Auto MDIX, the receive lines RXP and RXN require 6.8nF capacitors to filter the DC component, and only allow the AC signal to pass through to the PHY. R3 is set to 0 ohms to allow the RXP and RXN to set the DC component at the center tap of the magnetics. R7 and R8 are both left empty to disconnect the center tap and the external 3.3V from the RXP and RXN pins.

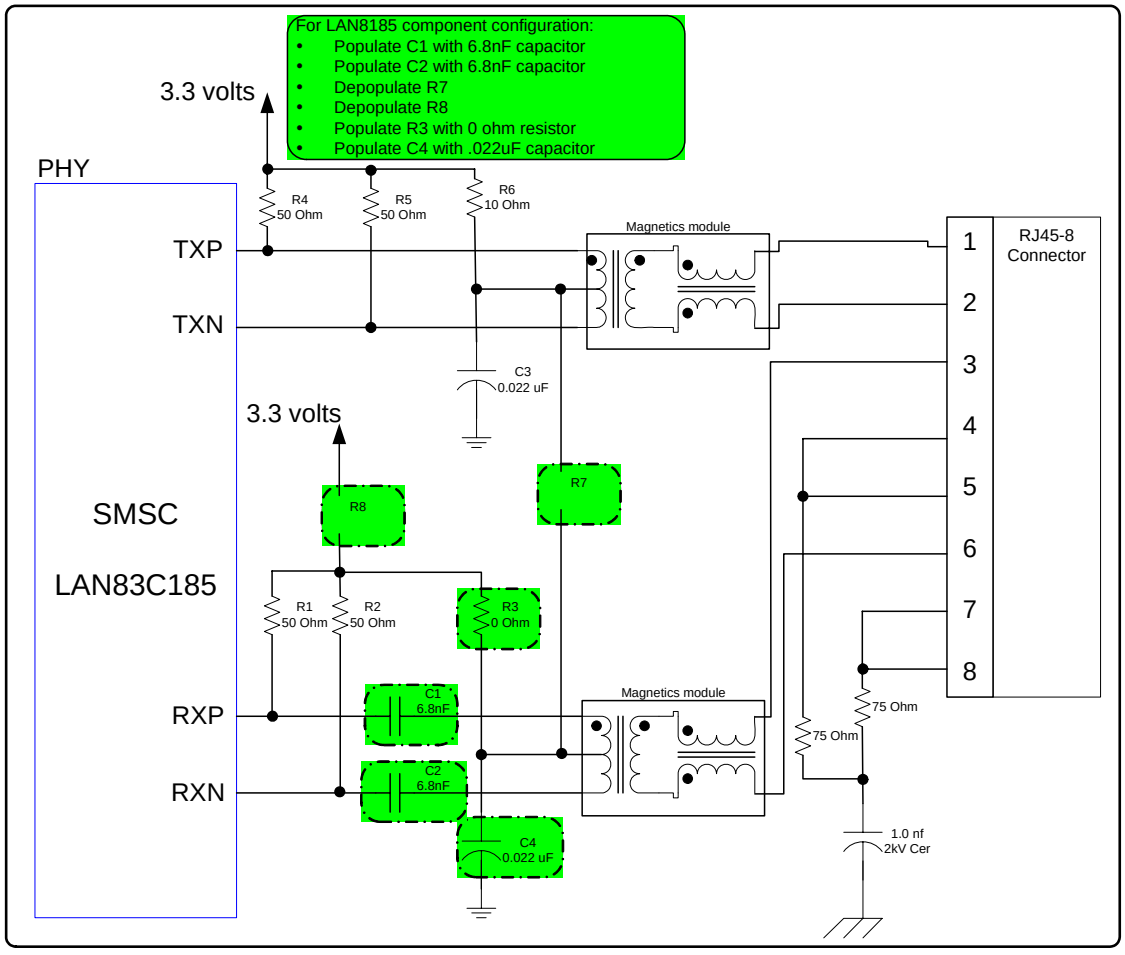

Figure 2.2 Scalable Design Configuration, Configured for LAN83C185 Operation, Non Auto MDIX

2.1.2 Scalable Design Configuration for HP Auto MDIX Mode

Figure 2.3 below illustrates the configuration for HP Auto MDIX with an SMSC LAN8187. The capacitor locations C1 and C2 must both be populated with 0 ohm resistors. Resistor R7 is populated with a 0 ohm resistor that connects the center taps of the transmit and receive magnetic modules together. Resistor R8 is populated with a 0 ohm resistor to bring the TX/RX pins up to 3.3 volts through a pair of 50 ohm resistors. Resistor R3 and capacitor C4 are de-populated in this configuration.

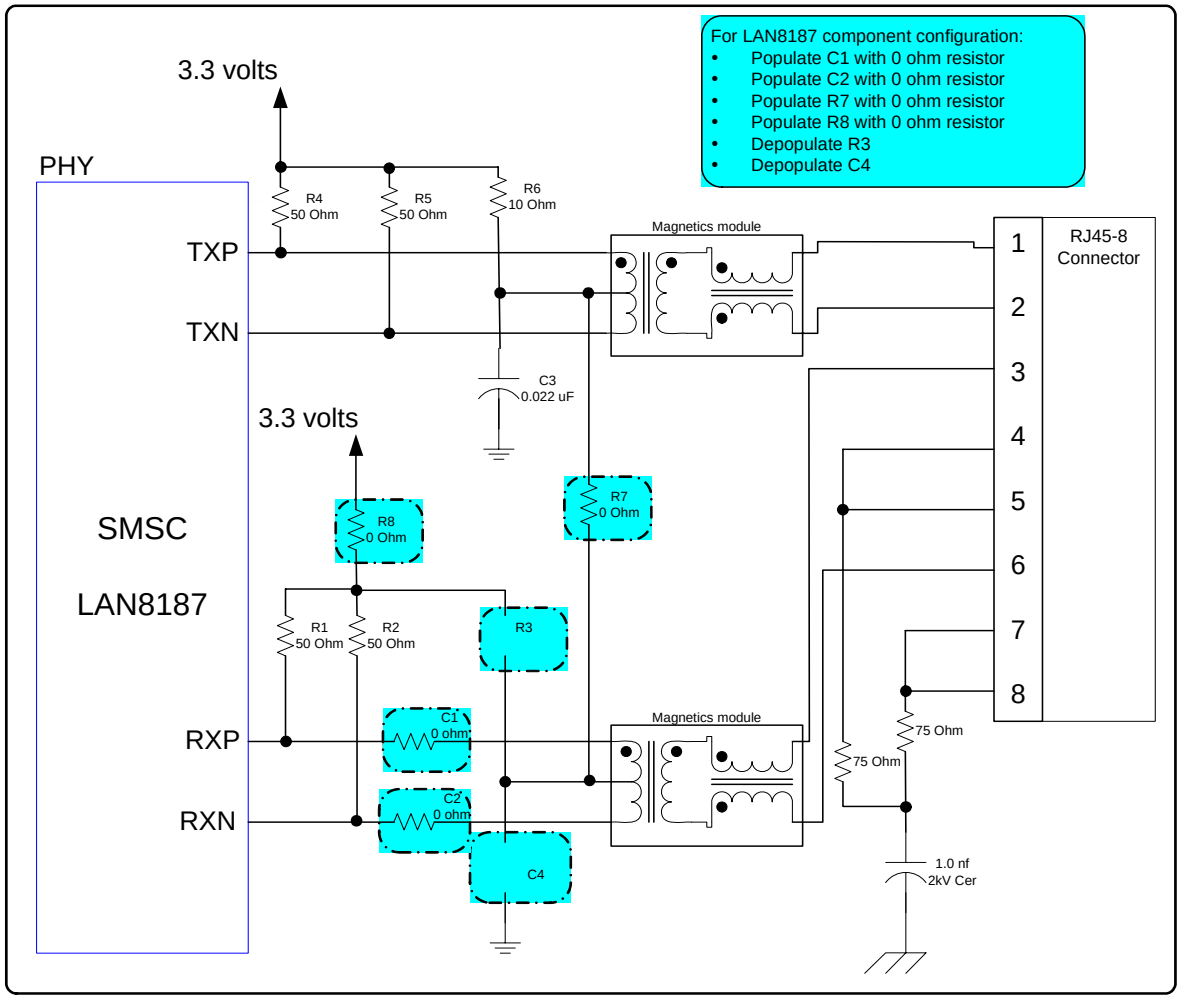

Figure 2.3 Scalable Design Configuration, Configured for HP Auto MDIX Operation with the LAN8187

2.2 Other Considerations

In order to transition from the LAN83C185 to the LAN8187, a few pins need some special consideration depending on usage options.

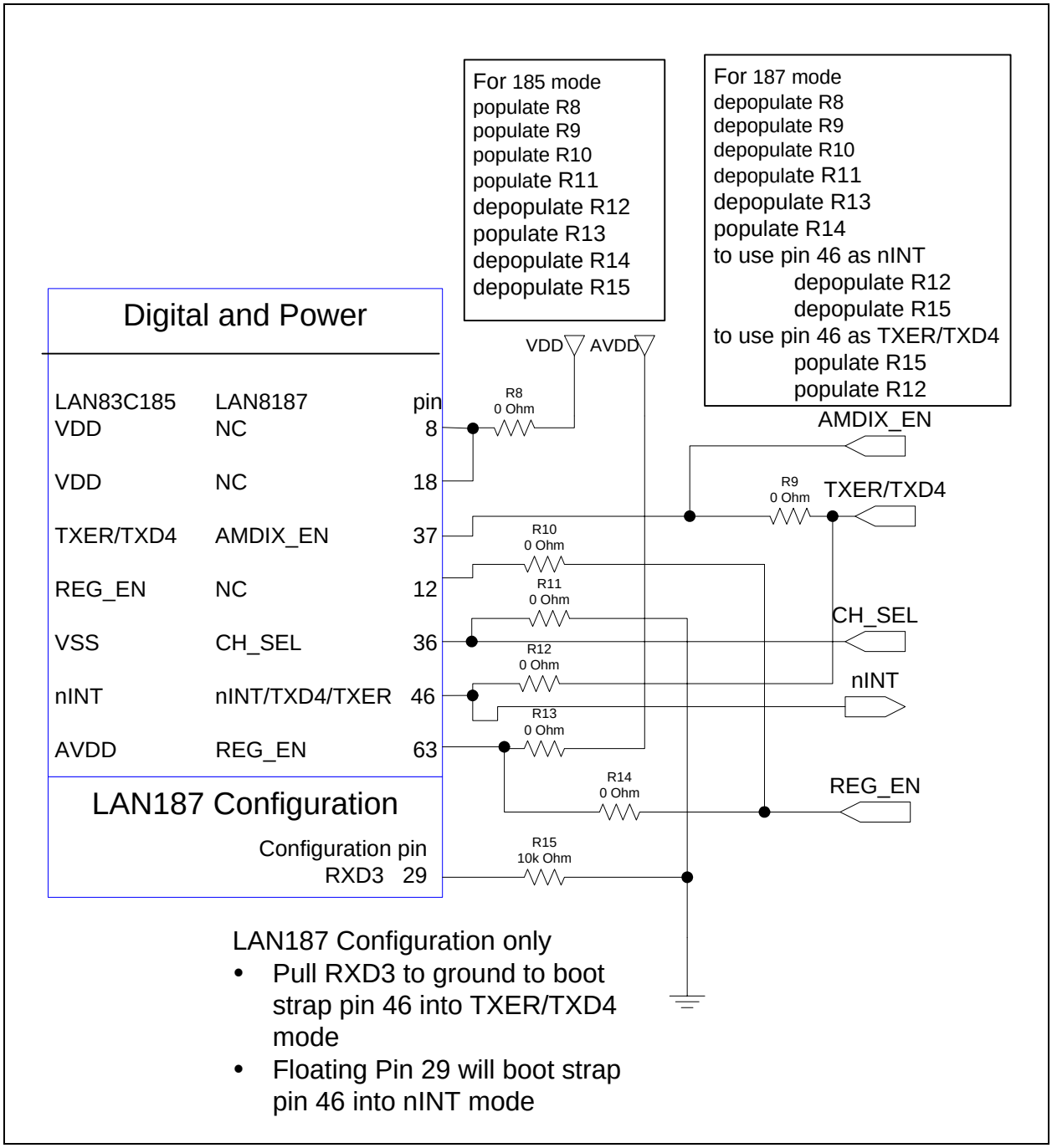

Figure 2.4 Other Considerations: Digital signals/configurations and power signals.

- **Power:** The number of power pins has been reduced from the LAN83C185 to the LAN8187. Pins 8 and 18 are VDD on the LAN83C185, but become No Connects on the LAN8187. Pin 36 is a VSS pin and becomes the Channel Select pin.

- **Signaling:** The TXER and TXD4 pin on the LAN83C185 is combined with the nINT pin on the LAN8187 to form the nINT/TXD4/TXER pin 46. This pin has two modes depending on the boot strapping option selected by pin 29 (RXD3).
  - If RXD3 is left floating, then it defaults pin 46 to nINT mode.
  - If RXD3 is pulled low by a 10k ohm resistor then it bootstrap configures pin 46 to TXER/TXD4 mode.
- **Internal Regulator:** The internal regulator enable pin moved from pin 36 to pin 63. For designs that don't want to turn off the internal +1.8v regulator, always leaving pin 63 to VDD will work for both LAN83C185 and LAN8187 configurations.
  - On LAN8187 configurations, attaching a 0 ohm resistor to pin 12 allows the designer to make pin 12 a no connect when switching to a LAN8187 design.
- **TXER/TXD4/AMDIX_EN:** Pin 37 has the role of a TXER/TXD4 and AMDIX_EN pin for the LAN83C185 and LAN8187 configurations.
  - Since AMDIX_EN is not available for a LAN83C185 configuration, populating R9 will tie the TXER/TXD4 of the system to the proper TXER/TXD4 pin on the PHY.

2.2.1 Other Considerations for LAN83C185 configuration

For LAN83C185 mode configuration, resistor R12, R14, and R15 are depopulated to connect the LAN83C185 digital signals to the appropriate system signals.

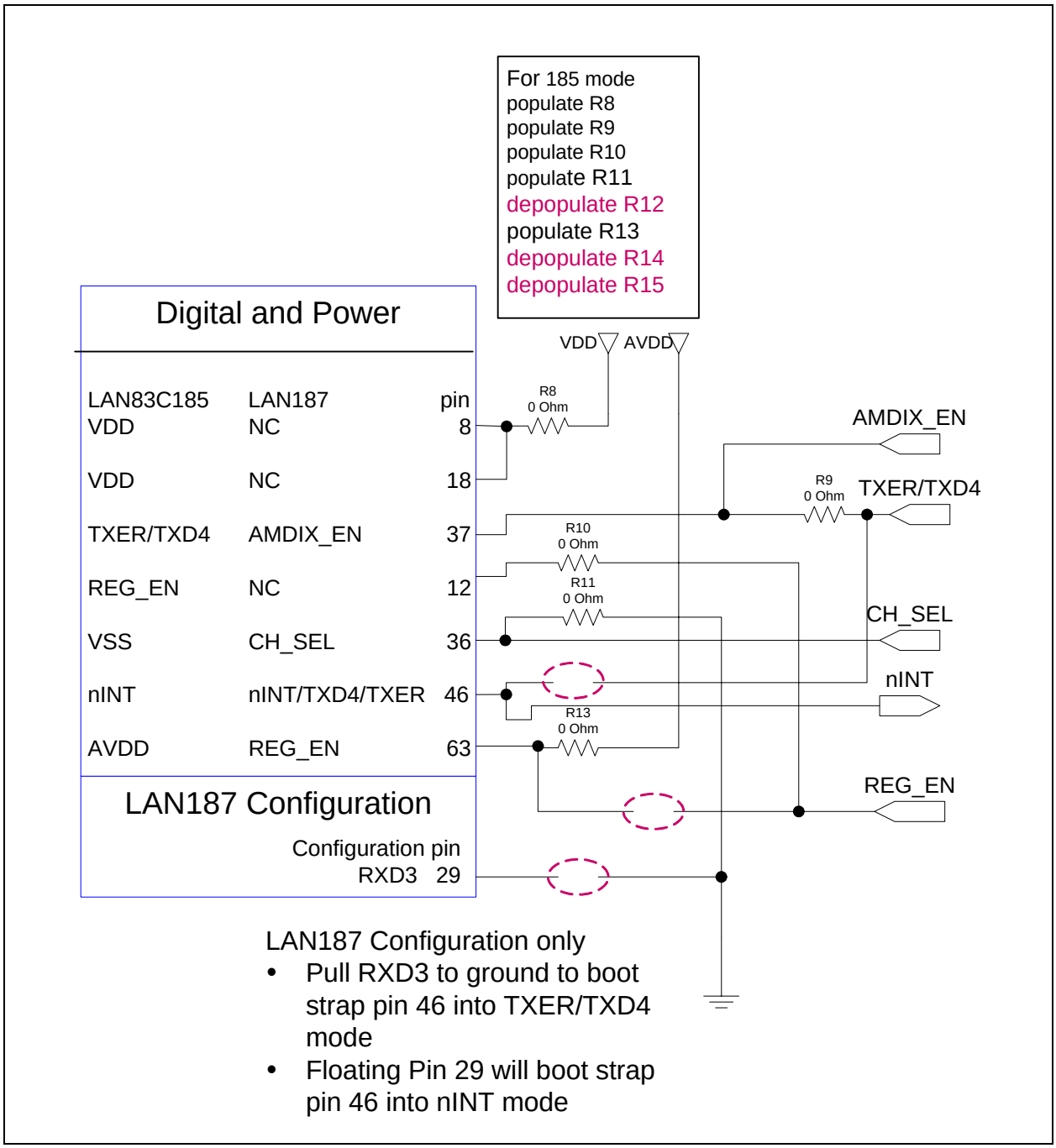

Figure 2.1 Other Considerations configured as a LAN185 in system.

2.2.2 Other Considerations for LAN8187 configuration

For the LAN8187 configuration, R8,R9, R10, R11, R13 are all depopulated to connect the pins to the appropriate system function. R12 and R15 are either populated or depopulated depending on the system designers needs.

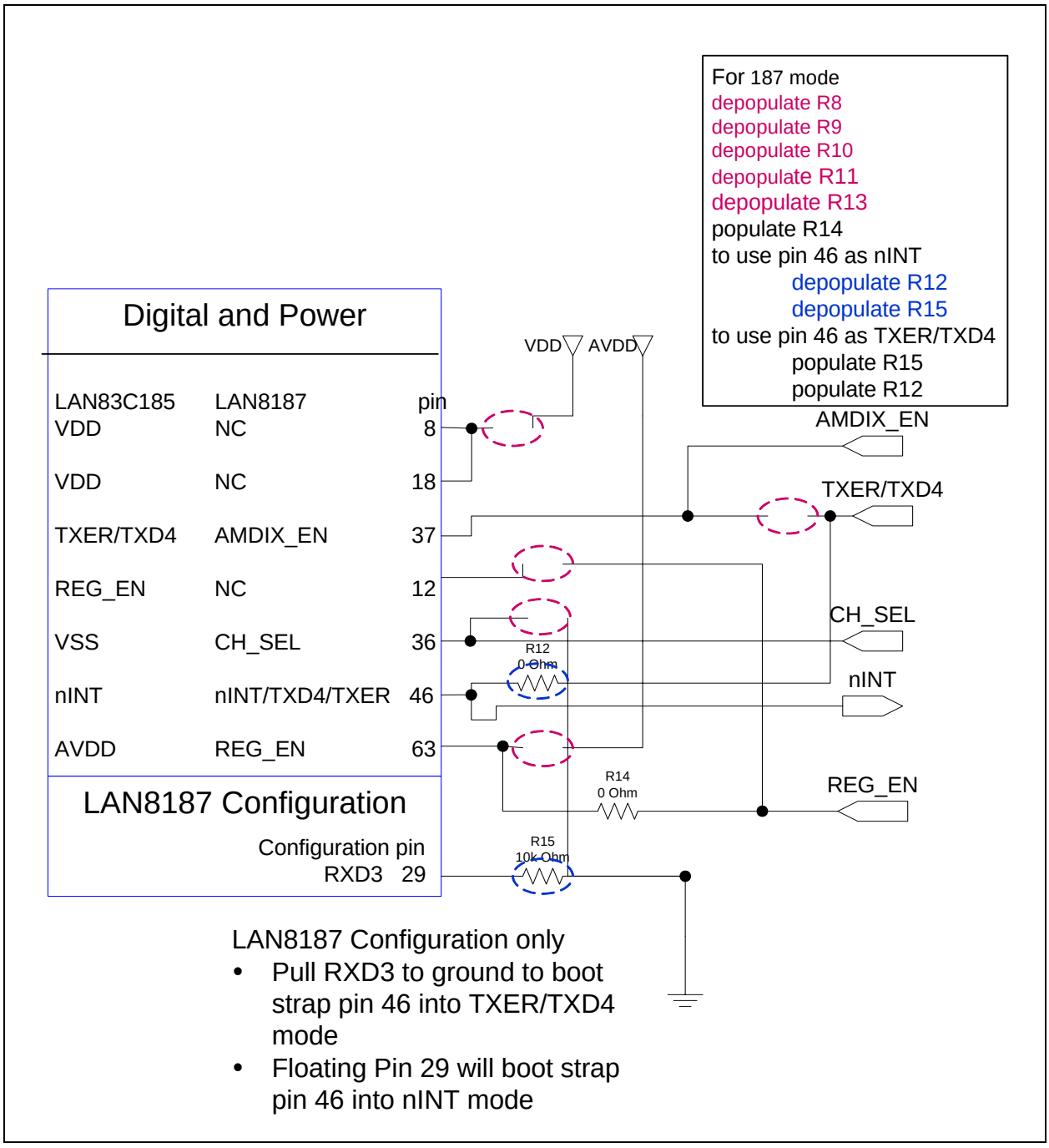

Figure 2.2 Other Considerations configured as a LAN8187 in system.

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