

XILINX CPLDs. THE COMPLETE CPLD SOLUTION.

The image is a collage featuring several Xilinx CPLD chips and their associated marketing terms. The chips shown include:

- XC9500**: A small green chip with the Xilinx logo and 'XC9500' printed on it.
- XC9500V**: A square black chip with the Xilinx logo, a blue lightning bolt, and 'XC9500V' printed on it.
- XC9500XL**: A square black chip with the Xilinx logo, an orange lightning bolt, and 'XC9500XL' printed on it.
- CoolRunner-II**: A square black chip with the Xilinx logo and 'CoolRunner-II' printed on it.
- CoolRunner**: A small green chip with the Xilinx logo and 'CoolRunner' printed on it.

The marketing terms scattered around the chips are:

- High Performance**: Located at the top left.
- DataGATE**: Located on the left side.
- Lowest Cost**: Located at the bottom left.
- CoolCLOCK**: Located at the bottom center.
- Low Power**: Located on the right side.

XILINX.

THE LEADER IN
PROGRAMMABLE LOGIC
SOLUTIONS.

Xilinx leads the industry in innovative programmable logic solutions, from our Virtex™ and Spartan™ FPGAs to our CPLDs. This breadth of products means you can get all of your programmable logic from one vendor, in one tool set, with one relationship.

Our CPLD portfolio includes the low-power, high-performance CoolRunner™ series and the low-cost XC9500 series.

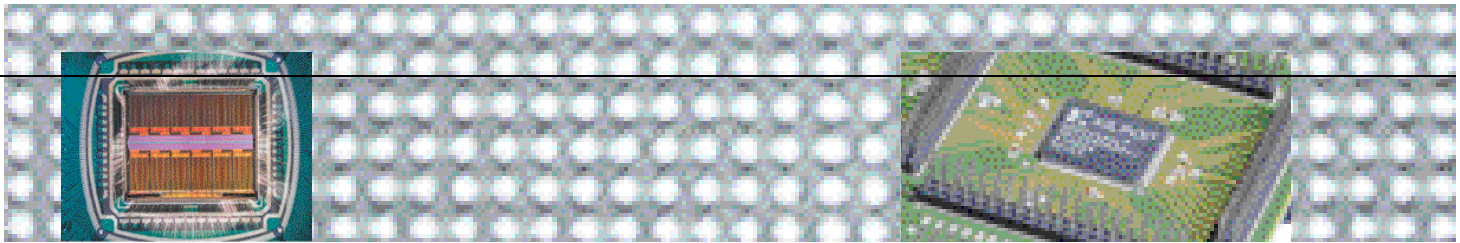
- The CoolRunner series (CoolRunner XPLA3 and CoolRunner-II™ families) features the lowest-power, highest-performance devices in the industry.

These CPLDs deliver advanced features to support system-level designs such as I/O banking, sophisticated clock control, and superb design security.

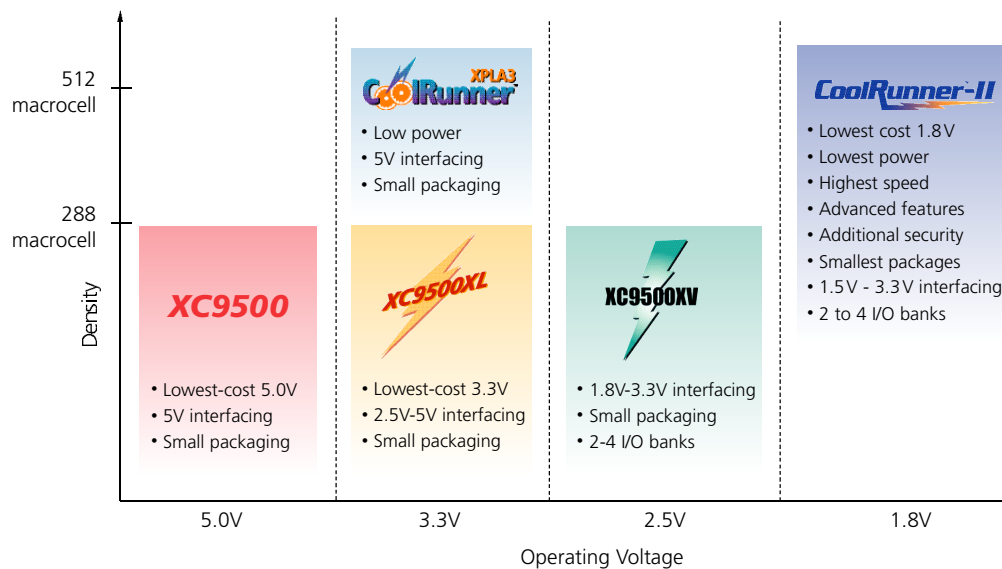
- The XC9500 series (XC9500, XC9500XL and XC9500XV families) offers the lowest cost and broadest range of I/O voltage support, and are ideal for integrating discrete logic, replacing obsolete components, and providing flexible programmability to digital systems.

Xilinx CPLD families comprise a complete portfolio of nonvolatile programmable logic devices. They are supported in a single design tool, and come complete with reference designs, access to IP, design services, development boards and excellent technical support—everything you need to complete your designs in record time and with minimum effort.





COMPLETE CPLD SOLUTIONS.



Xilinx offers high-quality, low-cost CPLDs for a wide range of high-volume applications, including:

Pb-free choices for:

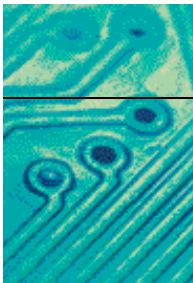
- CoolRunner-II
- CoolRunner XPLA3
- XC9500XV
- XC9500XL
- XC9500

Extended temperature ranges for:

- CoolRunner-II
- CoolRunner XPLA3
- XC9500XV
- XC9500XL
- XC9500

Xilinx programmable logic leadership ensures that you'll find a solution for every design challenge, whether you need low power, high performance, or a combination of the two. No other company offers you this range of choices.

Find out more at www.xilinx.com/cpld



REAL LOW-POWER PERFORMANCE. REAL VALUE. REALDIGITAL™ TECHNOLOGY.

The CoolRunner-II™ family of RealDigital CPLDs provides the low-power operation and cost-effective technology leadership you expect from Xilinx.

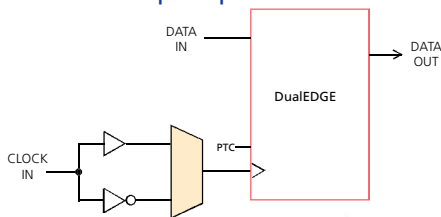
RealDigital technology delivers high performance without the sense amps traditionally used in CPLD product terms, making it the ideal low-power solution for battery-operated applications. For low cost and high performance, Xilinx manufactures CoolRunner-II CPLDs in 0.18-micron technology. Best of all, the CoolRunner-II family has an impressive array of features to make design easier and more integrated. You get the lowest cost, lowest power, best features, and highest performance—making the CoolRunner-II RealDigital family the ultimate CPLD solution.

					
Package Type:	QF32	CP56	QF48	VQ44	TQ100
Board Area:	25mm ²	36mm ²	49mm ²	144mm ²	256mm ²
Bottom View/Actual Size					

CoolRunner-II CPLDs are now available in the Micro Lead Frame package—the smallest form factor in the industry.

Find out more at www.xilinx.com/packages/qf

DualEDGE Flip-Flops



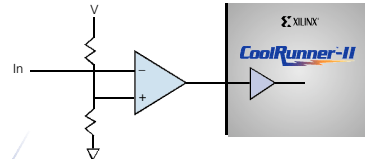
DualEDGE flip-flops for:

- Higher-resolution PWM
 - Motor control
 - Light intensity
 - LCD contrast
 - Power conversion
 - Position indication
- Faster conversions
 - Binary to BCD
- Synchronous communications
- Increased timer resolution

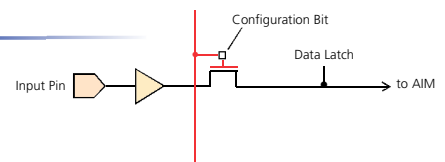
Advanced security minimizes the chance of design theft, making it ideal for cell phones, PDAs, and other wireless applications.

500mV input hysteresis for:

- Improved noise immunity
- Reduced power consumption
- Better signal integrity



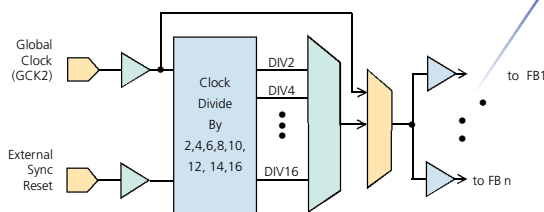
DataGATE



DataGATE for:

- Reducing power consumption
 - Internal control
 - External signal control
- Hot plugging
- System debugging
- Enhanced security

Clock Division



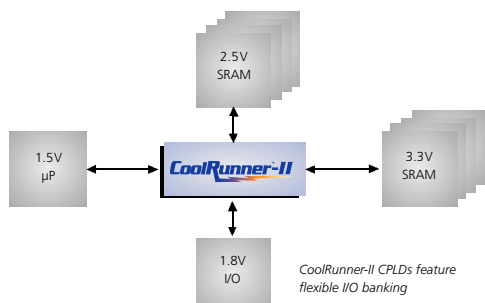
Clock Division for:

- Odd clock generation
- Duty cycle correction (50/50)
- Multiple clock trees

On The Fly (OTF) reconfiguration for:

- Two CPLDs for the price of one
- System function and FPGA configuration
- Board-level testing

System Voltage Integration



I/O banking for:

- System voltage integration

Find out more at www.xilinx.com/cr2

CPLD FLEXIBILITY, PERFORMANCE, AND VALUE.

CoolRunner XPLA3. Low Power with 5V I/O Tolerance.

The CoolRunner XPLA3 family of CPLDs is the right choice when you need a low-power CPLD with 5V I/O interfacing.

Portable, hand-held, and power-sensitive systems such as PDAs, digital cameras, and cell phones are ideal candidates for the many features of CoolRunner XPLA3 CPLDs:

- Less than 100 μ A standby current
- 5V I/O Tolerance
- 3.3V core voltage
- Up to 200 MHz performance
- Superior pin locking to allow designers to change their CPLD design without affecting board layout



Find out more at www.xilinx.com/cpld/xpla3

BILITY



XC9500 Series. Superior CPLD Performance and Flexibility.

The XC9500 CPLD series provides a wide range of density options—from 36 to 288 macrocells—as well as 2.5V, 3.3V, or 5V operation. You get a low-cost, highly reliable solution with a power-reduction mode.

XC9500XL CPLDs

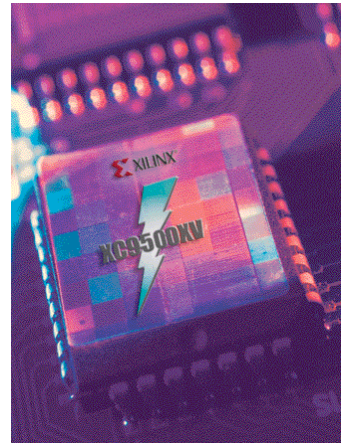
- 3.3V core voltage
- Lowest cost per macrocell
- 5.0V, 3.3V and 2.5V I/O interfacing
- Extended temperature ranges available for automotive applications

XC9500XV CPLDs

- 2.5V core voltage
- 2 to 4 I/O banks on higher densities
- 3.3V, 2.5V, 1.8V I/O interfacing
- Input hysteresis

XC9500 CPLDs

- 5.0V core voltage
- 5.0 V and 3.3 V I/O interfacing

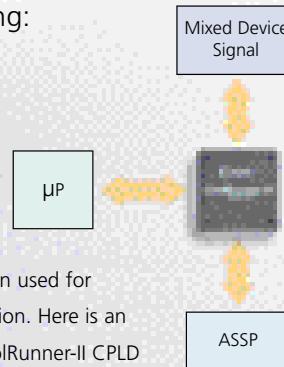


VALUE

THE MANY USES FOR XILINX CPLDs.

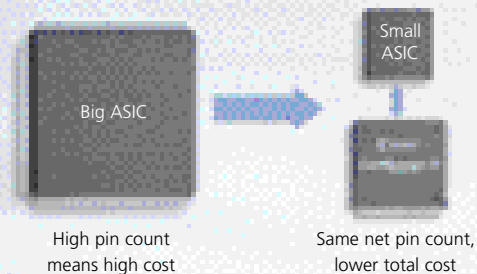
Xilinx CPLDs are used in many applications, including:

- Voltage-level translation
- Standard bus interface (I²C, SPI, 8b/10b)
- I/O expansion
- Microprocessor interface
- Bus transceivers
- Memory controllers
- ASIC patch
- Video clock generator
- Discrete logic replacement
- Display driver
- PAL/GAL consolidation
- State machine/control logic



Xilinx CPLDs are often used for voltage-level translation. Here is an example using a CoolRunner-II CPLD in a mobile phone.

Pin Expansion



Instead of using a costly high pin-count ASIC, use the same ASIC design in a smaller package—plus an inexpensive Xilinx CPLD—and get the same I/O, but at a much lower cost.

Our low-power CoolRunner-II and CoolRunner XPLA3 families allow designers to use programmable logic in:

- Digital cameras
- Wireless communicators, including mobile phones
- GPS transceivers
- Memory upgrades
- MP3 players
- Hand-held test and measurement equipment
- Hand-held medical instruments
- Inventory systems



Design Faster with CoolRunner Reference Designs.

Xilinx CPLD reference designs make designing much easier than with other solutions.

These drop-in, ready-to-use functions are comprised of HDL design code and application notes that allow you to finish your design faster. You can also increase product flexibility and user advantages with our comprehensive reference designs.

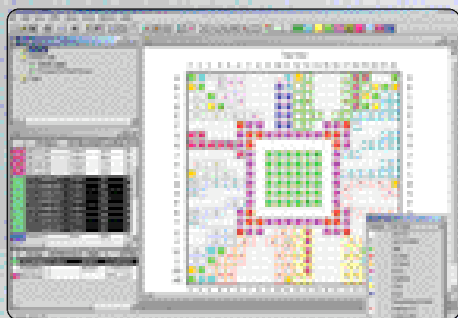
CPLD QuickStart Applications.

Xilinx CoolRunner-II and CoolRunner XPLA3 CPLDs are shown in a wide range of design examples—with presentations and demonstrations—to show how you can complete your design faster, with lower power and lower cost.

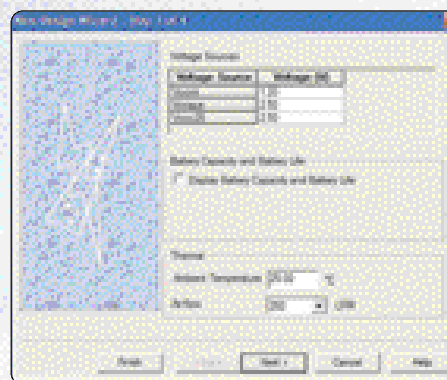
THE INDUSTRY'S EASIEST-TO-USE SOFTWARE.

The ISE WebPACK™ design tools offer the most complete, easy-to-use software solution for developing any Xilinx CPLD or medium-density FPGA design.

- Complete, downloadable, free CPLD desktop solution
- ABEL v7.5 synthesis and simulation
- State diagram entry
- HDL testbench generation
- 3rd-party simulation and EDA support
- Power-analysis software



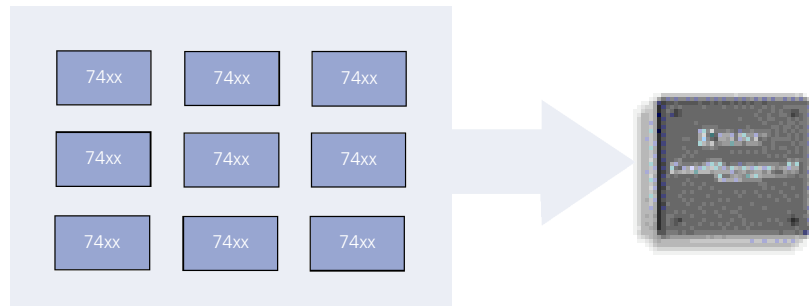
PACE helps simplify the pin management and area constraints definitions process.



XPower lets you estimate power requirements for your design early in the process.

Find out more at www.xilinx.com/ise/webpack

- Reduced component and manufacturing costs
- Reduced component count and PC board space
- Decreased time to market
- Increased reliability



The screenshot shows a Microsoft Excel window titled "Microsoft Excel - 1_xla_test6.xls". The application is running the "XILINX 7400 Conversion Calculator".

	A	B	C	D	E	F	G	H	I	J	K
1				7400 Conversion Calculator							
4	Please Select Category, Device & Total					Discrete	MacroCell Utilization				
6	Category	Device	Description	Total	Cost \$	CoolRunner	9500				
7	SSI_Gates	7455	2-Wide 4-Input AND-OR-INVERT Gate	1	0.18	1.0	1.0				
8	MUX_Gates	74445	BCD-To-Decimal Decoder/Driver	3	3.6	30.0	30.0				
9	Registers	74825N	8-Bit Bus Interface Flip-Flops With 3- State Outputs	4	1	32.0	32.0				
10	Driver_Rec	74467	Octal Buffers With 3-State Outputs	1	4.8	8.0	8.0				
11	Counters	74690	Synchronous Decade Counter With 0-9 Outputs	1	2	13.0	13.0				
12	Latches	74846	8-Bit Bus Interface D-Type Latches With 3- State Outputs	1	0.25	8.0	8.0				
13	Select Category			0	0	0.0	0.0				
14	Select Category			0	0	0.0	0.0				
15	Select Category			0	0	0.0	0.0				
16	Select Category			0	0	0.0	0.0				
17	Select Category			0	0	0.0	0.0				
18	Select Category			0	0	0.0	0.0				
19	Select Category			0	0	0.0	0.0				
20	Select Category			0	0	0.0	0.0				
21	Select Category			0	0	0.0	0.0				
22	Select Category			0	0	0.0	0.0				
23	Select Category			0	0	0.0	0.0				
24	Select Category			0	0	0.0	0.0				
25	Select Category			0	0	0.0	0.0				
26					Per Board	Discrete(s)	Est Macrocells*	Est Macrocells*			
27	Totals		Discrete Device Count	11	\$ 11.93	61.4	61.4				

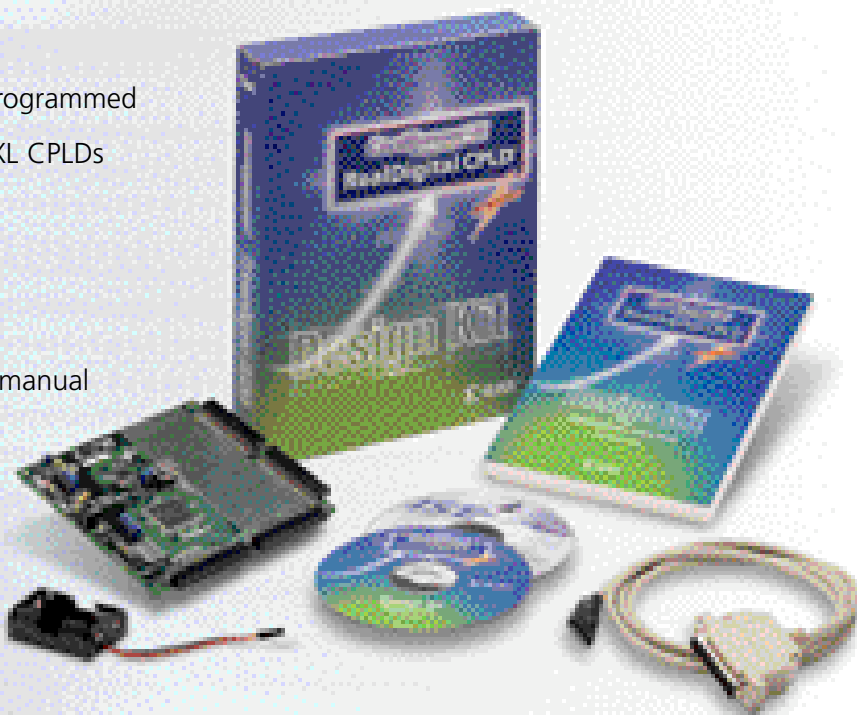
* Est Macrocell savings 10% reduction due to busio interface

Find out more at www.xilinx.com/cpld/logic-consolidator

TAKE THE NEXT STEP.

The Xilinx CPLD design kit contains everything you need to design and debug your next CPLD design, including:

- ISE WebPACK software
- Prototype board with pre-programmed CoolRunner-II and XC9500XL CPLDs
- Download cable
- Training material
- Resource CD with:
 - Schematics and reference manual
 - Links to reference designs
 - Application notes
 - Data sheets
 - Tutorials
 - QuickStart Seminars



Find more information on our complete line of CPLD solutions,
visit us online at www.xilinx.com/cpld/kit



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2005

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